REMARKS

By this Preliminary Amendment, claims 1, 3, 23 have been amended. Claims 34 and 35 have been added, however no new matter has been entered into the application. Claim 2 is canceled without prejudice or disclaimer of the subject matter therein. Claims 5, 7-10, 12-22, 24, and 26-30 have been previously canceled. No further claims have been added or canceled. Claims 1, 3, 4, 6, 11, 23, 25, and 31-33 are pending.

Applicant respectfully submits that the preliminary amendments presented herein expand upon those presented in the Response After Final Rejection submitted on September 14, 2006, which was not entered by the Examiner. No new matter has been added.

Regarding Comments of Advisory Action

In the Advisory Action mailed September 19, 2006, the Examiner objects to an added limitation in the amendments to claims 1 and 23. In particular, the Examiner asserts that the proposed amendment "forming source/drain regions proximate the first gate electrode and second gate electrode" is not disclosed in the original application after the step of patterning the first and second gate electrodes.

Responsive to the Examiner's comments, it is respectfully submitted that page 19, paragraph [0039], lines 14-17 of the original specification states "The resulting first and second transistors 610, 640, may then be subjected to conventional manufacturing techniques resulting in a device similar to the semiconductor device 100 illustrated in FIGURE 1". Note that Fig. 1 includes the source/drain regions. Further, page 8, lines 1-3 of paragraph [0020] and page 10, lines 5-6 of paragraph [0023] identify the

source/drain regions as conventional, and thus within the description of paragraph [0039] as described.

Accordingly, the claim limitation is fully supported in the original specification.

Rejection of Claims 1-4 Under 35 U.S.C. § 102(b)

In the Final Office Action, the Examiner rejected claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by *Rotondaro et al.* (U.S. Patent Publication No. 2003/0062577). This rejection is respectfully traversed.

Claim 1 is directed to a method for manufacturing a semiconductor device, comprising: forming a single layer metal gate electrode material over a semiconductor substrate, wherein the metal gate electrode material has a work function; subjecting at least a portion of the metal gate electrode material to at least one of a plasma silicidation or plasma germanidation process to cause the portion to be converted into a plasma altered metal gate electrode and have a different work function; patterning the metal gate electrode material having the work function and patterning the portion of the metal gate electrode material having the different work function to form a first gate electrode having the work function and a second gate electrode having the different work function; and forming source/drain regions proximate the first gate electrode and second gate electrode.

It is the Examiner's position that *Rotondaro et al.* meet the limitations of claim 1.

To the contrary, *Rotondaro et al.* require two layers of a metal material and deposition of the second silicon-germanium layer does not subject a single metal gate electrode material to a plasma process such that the subjecting causes the portion to be

converted into a plasma altered metal gate electrode and have a different work function. See, for example, paragraph [0017] thereof which states that the silicon-germanium layer 50 is formed over the metal layer 40. Further referring to paragraph [0018] thereof, the silicon-germanium layer 50 is a conformal layer that may be deposited by any suitable means, preferably ensuring little or no reaction between the silicon-germanium layer 50 and the metal layer 40. Even in view of a deposition of layer 50 with a plasma process, there will remain two distinct metal layers, 40 and 50 and deposition of layer 50 is not "subjecting" or causing the portion (of the single metal gate electrode material) to be converted into a plasma altered metal gate electrode and have a different work function as claimed.

For the above reasons, *Rotondaro et al.* fail to meet at least the claimed limitation of a single metal gate electrode material and subjecting at least a portion of the single metal gate electrode material to at least one of a plasma silicidation or plasma germanidation process to cause the portion to be converted into a plasma altered metal gate electrode and have a different work function.

Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 1-4 under 35 U.S.C. § 102(b). Applicant respectfully submits that remaining claims 3, 4 are in condition for allowance, at least by virtue of their dependency from allowable claim 1, respectively.

Rejection of Claims 1 and 6 Under 35 U.S.C. § 102(e)

In the Final Office Action, the Examiner rejected claims 1 and 6 under 35 U.S.C. §102(e) as being anticipated by *Woo et al.* (U.S. Patent No. 7,071,086). This rejection is respectfully traversed.

The subject matter of claim 1 remains as described above.

It is the Examiner's position that *Woo et al.* disclose all limitations of claim 1, referring to Figs. 3B, 4B and column 3 to column 5, line 25 of *Woo et al.* for support of this position.

To the contrary, it is respectfully submitted that column 4, line 66 – column 5, line 3 of *Woo et al.* include disclosure explaining that a metal gate is formed of two layers as opposed to the single layer claimed. More specifically, the disclosure states "[f]ollowing the deposition of the metal layer 28, a planarization process, such as a chemical mechanical planarization (CMP), is performed to create the metal gate 30 comprising the metal layer 28 and the metal layer 26 with the incorporated silicon". Thus, to obtain a metal gate electrode *per se*, requires two metal layers instead of the single metal layer as claimed.

Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 1 and 6 under 35 U.S.C. § 102(e). Applicant submits that claim 6 is further in condition for allowance at least by virtue of its dependency from allowable claim 1.

Rejection of Claims 1, 2, 6 and 11 Under 35 U.S.C. § 103(a)

In the Final Office Action, the Examiner rejected claims 1, 2, 6, and 11 under 35 U.S.C. §103(a) as being unpatentable over *Wilk et al.* (U.S. Patent No. 6,291,282) in view of *Woo et al.* (U.S. Patent No. 7,071,086). This rejection is respectfully traversed.

The subject matter of claim 1 remains as described above.

It is the Examiner's position that Figs. 3d-3e and column 4, line 4 to column 5, line 49 of *Wilk et al.* disclose all but the step of subjecting at least a portion of the metal gate electrode material to at least one of a plasma silicidation or plasma germanidation process, which is a limitation of independent claim 1. The Examiner has applied *Woo et al.* as incorporating silicon into a metal layer to control the work function of a metal gate layer, referring to column 4, lines 52-54 thereof.

To the contrary, it is respectfully submitted that while *Woo et al.* appear to describe a silane plasma treatment, there is no teaching or suggestion that this treated material is a "single metal gate electrode material" as claimed. Instead, as identified at column 5, lines 1-3 of *Woo et al.*, CMP is performed to create the metal gate 30 comprising the metal layer 28 and the metal layer 26 with the incorporated silicon. Thus, the silicon incorporated layer does not meet at least the claim limitation of forming a single layer metal gate electrode material over a semiconductor substrate, or further subjecting at least a portion of the single layer metal gate electrode material to the claimed plasma process.

Accordingly, while *Woo et al.* disclose plasma silane treatment in connection with a metal layer, this treatment is not of the single layer metal gate electrode material as claimed. Given the requirement of two metal layers to form a gate electrode in *Woo et*

al., one would not be motivated to combine such a process with the structure of *Wilk et al.* to render the claimed invention.

Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 1, 2, 6 and 11 under 35 U.S.C. § 103(a). Applicant submits that claims 2, 6 and 11 are further in condition for allowance at least by virtue of their dependency from allowable claim 1.

Rejection of Claims 23, 25, 31 Under 35 U.S.C. § 103(a)

In the Final Office Action, the Examiner rejected claims 23, 25, 31 under 35 U.S.C. §103(a) as being unpatentable over *Wilk et al.* (U.S. Patent No. 6,291,282) in view of *Woo et al.* (U.S. Patent No. 7,071,086) and *Zhu et al.* (U.S. Patent No. 6,133,079). This rejection is respectfully traversed.

Claim 23 is directed to a method for manufacturing an integrated circuit, comprising: forming transistors over a semiconductor substrate, including; forming a single layer metal gate electrode material over the semiconductor substrate, wherein the metal gate electrode material has a work function; subjecting at least a portion of the metal gate electrode material to at least one of a plasma silicidation or plasma germanidation process to cause the portion to be converted into a plasma altered metal gate electrode and have a different work function; and patterning the metal gate electrode material having the work function and patterning the portion of the metal gate electrode material having the different work function to form a first gate electrode having the work function and a second gate electrode having the different work function;

forming source/drain regions proximate the first gate electrode and second gate electrode; and forming interconnects within dielectric layers located over the transistors.

It is the Examiner's position that Figs. 3d-3e and column 4, lines 4 to column 5, lines 49 of *Wilk et al.* disclose the features of claim 23 with the exception of subjecting at least a portion of the metal gate electrode material to at least one of a plasma silicidation or plasma germanidation process, or forming interconnects within dielectric layers located over the transistors. *Woo et al.* are applied for the first of these omissions and *Zhu et al.* are applied for forming interlevel dielectric and inter metal dielectric layers.

To the contrary, it is respectfully submitted that while *Woo et al.* appear to teach a silane plasma treatment, there is no teaching or suggestion that the treated material is a "single metal gate electrode material" as claimed. Instead, as identified at column 5, lines 1-3 of *Woo et al.*, CMP is performed to create the metal gate 30 comprising the metal layer 28 and the metal layer 26 with the incorporated silicon. Thus, the silicon incorporated layer does not meet at least the claim limitation of forming a single layer metal gate electrode material over a semiconductor substrate, or further subjecting at least a portion of the single layer metal gate electrode material to the claimed plasma process.

Accordingly, while *Woo et al.* disclose plasma silane treatment in connection with a metal layer, this treatment is not of the single layer metal gate electrode material as claimed. Given the requirement of two metal layers to form a gate electrode in *Woo et al.*, one would not be motivated to combine such a process with the structure of *Wilk et*

al. Further, the ILD and IMD layers of *Zhu et al.* do not overcome the missing teachings identified herein.

Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 23, 25 and 31 under 35 U.S.C. § 103(a). Applicant submits that claims 25 and 31 are further in condition for allowance at least by virtue of their dependency from allowable claim 23.

Rejection of Claims 23, 32-33 Under 35 U.S.C. § 103(a)

In the Final Office Action, the Examiner rejected claims 23, 32-33 under 35 U.S.C. §103(a) as being unpatentable over *Rotondaro et al.* (U.S. Patent Publication No. 2003/0062577) in view of *Zhu et al.* (U.S. Patent No. 6,133,079). This rejection is respectfully traversed.

The subject matter of independent claim 23 remains as described above and it is the Examiner's position that *Rotondaro et al.* meet the limitations of claim 23 with the exception of forming interconnects within dielectric layers located over the transistors. *Zhu et al.* are applied in combination with *Rotondaro et al.* as disclosing interconnects.

To the contrary, *Rotondaro et al.* require two layers of a metal material and deposition of the second silicon-germanium layer does not subject a single metal gate electrode material to a plasma process such that the subjecting causes the portion to be converted into a plasma altered metal gate electrode and have a different work function. *See*, for example, paragraph [0017] thereof which states that the silicon-germanium layer 50 is formed over the metal layer 40. Further referring to paragraph [0018] thereof, the silicon-germanium layer 50 is a conformal layer that may be deposited by

any suitable means, preferably ensuring little or no reaction between the silicon-germanium layer 50 and the metal layer 40. Even in view of a deposition of layer 50 with a plasma process, there will remain two distinct metal layers, 40 and 50 and deposition of layer 50 is not "subjecting" or causing the portion (of the single metal gate electrode material) to be converted into a plasma altered metal gate electrode and have a different work function as claimed.

For the above reasons, *Rotondaro et al.* fail to meet at least the claimed limitation of a single metal gate electrode material and subjecting at least a portion of the single metal gate electrode material to at least one of a plasma silicidation or plasma germanidation process to cause the portion to be converted into a plasma altered metal gate electrode and have a different work function.

Further, the ILD and IMD layers of *Zhu et al.* do not overcome the missing teachings identified with respect to *Rotondaro et al.*

Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 23, 32-33 under 35 U.S.C. § 103(a). Applicant submits that claims 32-33 are further in condition for allowance at least by virtue of their dependency from allowable claim 23.

CONCLUSION

If the Examiner believes that additional discussion or information might advance prosecution of the instant application, the Examiner is invited to contact the undersigned at the telephone number listed below to expedite resolution of any outstanding issues.

In view of the foregoing remarks, Applicant submits that this claimed invention, as amended, is neither anticipated nor rendered obvious in view of the references cited against this application. Applicant therefore requests the entry of this Amendment, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 20-0668.

Respectfully submitted,

Dated: December 18, 2006

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